ANALOG DEVICES

Low Cost 3½ Digit DPM For OEM Applications

AD2010

FEATURES
LED Display with Latched Digital Outputs
Small Size, Lightweight
Automatic Zero Correction; Max Error: 0.05% ±1 Digit
High Normal Mode Rejection: 40dB @ 50 or 60Hz
Optional Ratiometric Operation
Leading "0" Display Blanking
5V dc Powered

APPLICATIONS
Medical/Scientific/Analytic Instruments
Data Acquisition Systems
Industrial Weighing Systems
Readouts in Engineering Units
Digital Thermometers

GENERAL DESCRIPTION
Analog Devices' model AD2010 represents an advance in price/
performance capabilities of 3½ digit digital panel meters. The
AD2010 offers 0.05% ±1 digit maximum error with bipolar,
single ended input, resolution of 100μV, and a common mode
rejection ratio of 60dB (CMRR) at ±200mV (CMV).

The AD2010 features a light-emitting-diode (LED) display
with a full scale range of 0 to ±199.9 millivolts, latched digital
data outputs and control interface signals, and leading zero dis-
play blanking. Automatic-zero correction circuitry measures
and compensates for offset and offset drift errors, thereby
providing virtually no error. Another useful feature of the
AD2010 is its 5V dc operation. The AD2010 can operate from
the users' 5V dc system supply, thereby eliminating the shield-
ing and decoupling needed for line powered units when the ac
line must be routed near signal leads.

To satisfy most application requirements, the conversion rate
of the AD2010 is normally 4 readings per second. However, an
external trigger may be applied to vary the sampling rates from
a maximum of 24 readings per second down to an indefinite
hold time. The AD2010 can also be connected for automatic
conversion at its maximum conversion rate. During conversion,
the previous reading is held by the latched logic. The numeric
readout is available as BCD data. Application of the metering
system in a computer or data logging system is made easy with
the availability of the "overrange," "polarity," "overload,"
and "status" signals.

The AD2010/R option for ratiometric operation allows read-
ings to be made of the ratio of two input voltages as well as
the absolute value of the input. AD2010/R operation is de-
scribed in a later section.

A simplified block diagram of the AD2010, illustrating the
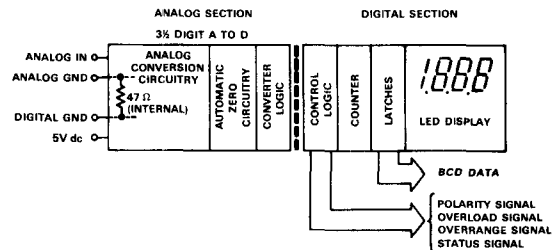features described above is shown in Figure 1.

Figure 1. Simplified Block Diagram

IMPROVED NOISE IMMUNITY, ACCURACY AND ZERO STABILITY
Dual-slope integration, as used in the AD2010 and as described
in the theory of operation section, offers several design benefits.
● Conversion accuracy, for example, is independent of both
the timing capacitor value and the clock frequency, since
they affect both the up ramp and down ramp integration
in the same ratio.
● Normal mode noise at line frequencies or its harmonics is
rejected since the average value of this noise is zero over the
integration period.
● To achieve zero stability, a time interval during each conver-
sion is provided to allow the automatic-zero correction cir-
cuitry to measure and compensate for offset and offset drift
errors, thereby, providing virtually no zero error.

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SPECIFICATIONS (typical @ +25°C and +5VDC unless otherwise noted)

DISPLAY OUTPUT
- Display consists of four LED's (7 segment – 0.27" (6.9mm) high). for data digits plus 100% overrange and polarity indication.
- Overload – three data digits display zeros and flashes.
- Decimal Points – selectable at input connector.
- Leading "0" Display Blanking – controlled externally.

INPUT
- Full Scale Range – 0 to ±199.9 millivolts
- Automatic Zero
- Automatic Polarity
- Bias Current – 3nA
- DC Impedance – 100MΩ
- Overvoltage Protection – 20V sustained, 50V momentary without damage.
- Decimal Points (3) – illuminate with logic "1", extinguish with logic "0".

ACCURACY
- Maximum Error – 0.05% of reading ±1 digit
- Resolution – 0.1 millivolt
- Temperature Range – 0 to +50°C operating
                      –30°C to +85°C storage
- Temperature Coefficient – ±50ppm/°C

NORMAL MODE REJECTION
- 40dB @ 60Hz (50Hz on AD2010/E)

COMMON MODE REJECTION
- 60dB @ ±200mV

CONVERSION RATE
- External Trigger – up to 24 conversions per second
- Internal Trigger – 4 conversions per second
- Automatic – A new conversion is initiated automatically upon completion of conversion in process; conversion rate will vary from 24/sec to 40/sec depending on input magnitude.
- Hold and Read upon command.

CONVERSION TIME
- Normal Conversion – 42ms max (full scale input)
                       50ms max Model AD2010/E
- Overload Conversion – 62ms max

INTERFACE SIGNALS
- DTL/TTL Compatible

	IN	OUT
logic "0"	<0.8V	<0.4V
logic "1"	>2.0V	>2.4V

- Inputs

External Trigger – Operation in the "External Trigger" mode requires that the "External Hold" input be a logic "0" or ground.

Negative Trigger Pulses – Applying a logical "low" to the "HOLD" input disables the internal trigger. A negative trigger pulse (logic "1" to logic "0") of 1.0μs minimum applied to the "EXT TRIGGER" input will initiate conversion in the same manner as the internal oscillator. The external trigger should not be repeated, however, until the "status" indicates completion of the conversion in process.

Positive Trigger Pulses – The "HOLD' input can be used to trigger the AD2010 from a "normally low" signal with the "EXT TRIGGER" input open or logic "1". Following a "hold" a new reading will be initiated on the leading edge of the "hold" signal. Thus, a momentary positive pulse on the "HOLD" input can be used to trigger the AD2010. The drift correct interval, however, begins on the trailing edge of the positive pulse, so if the pulse width exceeds 1ms, the conversion will actually be initiated by the internal trigger.

Maximum Conversion Rate - Automatic – The AD2010 can also be connected for automatic conversion at its maximum conversion rate by connecting the "status" output back into the "hold" input. In this manner the status signal going high at the end of one conversion immediately initiates a new conversion. The pulses appearing on the status line can be used to step a multiplexer directly, since the built-in drift-correct delay of 8.33ms will allow settling of the input prior to conversion. A logic "0" applied to the "EXT TRIGGER" will inhibit the automatic trigger mode.

External Hold – Logic "0" or ground applied to this input disables the internal trigger and the last conversion is held and displayed. For a new conversion under internal control the input must be opened or at logic "1". For a new conversion under external control, a positive pulse of less than 1.0ms can be applied (as previously explained).

OUTPUTS
- 3 BCD Digits (8421 Positive True) - latched - 3TTL loads
- Overrange - logic "1" - latched - 6TTL loads, indicates overrange.
- Overload - logic "0" indicates overload (>199.9mV) logic "1" - latched - 6TTL loads, indicates data valid.
- Polarity - logic "1" - latched - 6TTL loads, indicates positive polarity input.
- Status - logic "0" - conversion in process logic "1" - latched - 6TTL loads, indicates conversion complete.

POWER
- +5V dc ±5%, 500mA

WARM UP
- Essentially none to specified accuracy

ADJUSTMENTS
- Range potentiometer for full scale calibration. Calibration recommended every six months.
- Normal Mode Rejection potentiometer (AD2010R only)

SIZE
- 3"W x 1.8"H x 0.84"D (76.2 x 45.7 x 21.3mm) (overall depth for case and printed circuit board extension is 1.40" (35.6mm)).

ORDERING GUIDE
- AD2010 - Standard AD2010 as described above - tuned for peak normal mode rejection at 60Hz and its harmonics.
- AD2010/E - Standard AD2010 as described above - tuned for peak normal mode rejection at 50Hz and its harmonics.
- AD2010/R - Standard AD2010 as described above - with Ratiometric option.
- AD2010/E/R - Standard AD2010/E as described above with Ratiometric option.

WEIGHT
- 4 oz. (113.5gm)

CONNECTOR RECOMMENDATION
- 30 Pin 0.156 spacing, Viking No. 2Vk 15D/1-2 or Cinch type 251 No. 5030A30.
- Optional - Order AC1501.

Specifications subject to change without notice.

5V dc OPERATION PROVIDES REDUCED NOISE PICKUP, IMPROVES RELIABILITY

A DPM designed for 5V dc operation offers the user many advantages over ac line powered devices. These benefits include:

● REDUCED NOISE PICKUP AND SUSCEPTIBILITY. Since line voltages are not required for operation, signal leads and internal circuitry need not be exposed to this source of noise, thereby, reducing power-frequency interference. A separate 5V dc power supply also provides additional isolation from line transients. Shielding and decoupling of the DPM circuits can also be eliminated. The DPM may be used as a component without danger of shock hazards to operational personnel or nearby circuitry.

● IMPROVED RELIABILITY. DPMs without power supplies generally require less space and generate less heat. The result is improved reliability while achieving lower cost. The smaller package size provides greater packaging flexibility and requires less ventilation behind the panel.

LEDs GIVE LONG LIFE, SHARP DISPLAY

The numeric outputs are displayed using 0.27" high, 7 segment, red LEDs. The LEDs provide the physical ruggedness typical of ICs, with a life expectancy in excess of 100,000 hours. The displayed numerals are sharp and easily readable at distances of up to 8 feet. The clean uncluttered look of the lens and case design further enhance the visual attractiveness of the display.

Optical features of the display include: a minimum photometric brightness of 200 foot-lamberts, and a 6300 angstrom, wavelength at peak emission (red). Other display features include programmable decimal points, automatic zero, 4 readings per second display rate, external trigger-and-hold rate of up to 24 readings per second, flashing-zeros overload indication, and leading "zero" display blanking.

COMPACT DESIGN FEATURES EASY SNAP-IN INSTALLATION

The AD2010 is housed in an aluminum case providing light weight, structural strength, optimum heat dissipation and shielding against external noise. With overall dimensions as shown in Figure 6, minimum space is required both on the panel and behind it. No tools are required for installation. You simply snap in the case, then snap on the filter and lens. Its light weight makes AD2010 ideal for applications in hinged panel equipment.

THEORY OF OPERATION

The AD2010 (Timing Diagram Figure 7) uses a dual-slope integrating A/D conversion scheme. When an input signal is applied to the DPM, it is applied to an integrator at the same time a counter is activated, initiating the count of clock pulses. After a predetermined number of counts (a fixed interval of time, T), the polarity of the input signal is strobed and a reference voltage having opposite polarity is applied to the integrator. At this instant, the accumulated charge on the integrating capacitor, C, is proportional to the average value of the input over the interval T. The integral of the reference is an opposite-going ramp having the fixed slope V_{REF}/RC. At the same time, the counter is again counting from zero. When the integrator output reaches zero, the count is stopped, and the analog circuitry is reset. Since the charge gained is proportional to $V_{IN}T$, and the equal amount of charge lost is proportional to $V_{REF}/\Delta t$, then the number of counts relative to the full count is proportional to $\Delta t/T$, or V_{IN}/V_{REF}. The output of the counter is a BCD number, which is decoded and displayed as the digital representation of the input.

AD2010/R OPTION EXPANDS APPLICATION

RATIOMETRIC OPERATION WITH EXTERNAL REFERENCE: The ratiometric option (AD2010/R) allows readings to be normalized to an external reference. This option can be useful where the analog voltage to be measured is accurate relative to an external reference which in itself is not accurate. A ratiometric application is illustrated in Figure 2. In this example, a position readout potentiometer operates with an external excitation supply which itself may not be very accurate. However, the potentiometer output relative to the reference supply, will be accurate due to the potentiometric configuration.
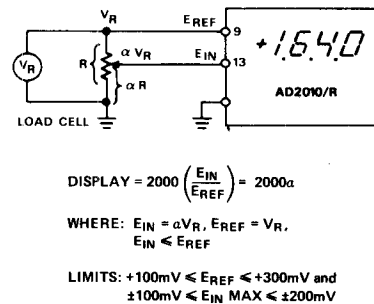

$$DISPLAY = 2000 \left(\frac{E_{IN}}{E_{REF}} \right) = 2000\alpha$$

$$WHERE: \ E_{IN} = \alpha V_R, \ E_{REF} = V_R,$$
$$E_{IN} \leqslant E_{REF}$$

$$LIMITS: +100mV \leqslant E_{REF} \leqslant +300mV \ and$$
$$\pm 100mV \leqslant E_{IN} \ MAX < \pm 200mV$$

Figure 2. Ratiometric Operation

In the AD2010 the normal reference voltage is 200mV and is internally connected. The AD2010/R, however, has a "Reference Input" where an external reference voltage in the range of 100-300mV can be applied. The displayed output is given by:

$$Display = 2000 \left(\frac{E_{IN}}{E_{REF}} \right)$$

The AD2010 also has a "Reference Output" where the normal 200mV reference is available. Absolute measurements using the AD2010/R can be made by externally connecting "Reference Output" to "Reference Input." The "Reference Output" is provided for this purpose only. It should be noted that the ratiometric option is intended only for normalization, and that the external reference must be a steady dc voltage.

INTERFACING THE DPM

The AD2010 can also be connected for automatic conversion at its maximum conversion rate by connecting the "status" output (Pin K) back into the "hold" input (Pin D). The 70ns pulses appearing on the status output line may be used to step a multiplexer. The status pulse width may be increased (if desired) as shown in Figure 3.
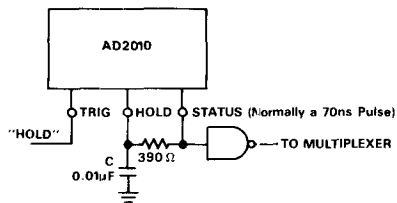
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AD2010

○ TRIG ○ HOLD ○ STATUS (Normally a 70ns Pulse)

"HOLD"

C
0.01µF   390Ω   ○— TO MULTIPLEXER

Figure 3. Increasing Pulse Width for Multiplexer Control in the Automatic Mode

To maximize the common mode rejection, an external 100µF @ 3V capacitor, C, is recommended as illustrated in Figure 4. The capacitor will reduce ground noise and ripple where the interconnection wires are 12 inches or longer. The polarization of C will depend on actual configuration.

AD2010

47Ω

INPUT ○ ANALOG GND ○ DIG GND (BCD) ○ +5V ○ 0V ○
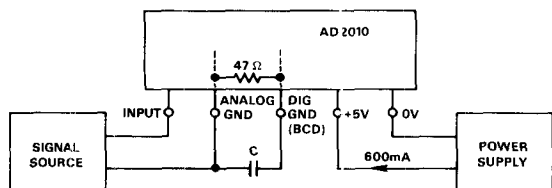
C

SIGNAL SOURCE

600mA

POWER SUPPLY

Figure 4. Insuring Maximum Common Mode Voltage Rejection

The latched digital data outputs and control interface signals are available at the rear of the AD2010. The signals may be interfaced with the system using a Cinch or Viking PC edge connector with 0.156" spacing or the AC1501 connector option. Signal and pin designations are shown in Figure 5.

PIN REF	PIN FUNCTION	PIN REF	PIN FUNCTION
1	EXTERNAL TRIGGER	A	1000's DIGIT (OVERRANGE)
2	800's DIGIT	B	100's DIGIT
= KEY			
3	400's DIGIT	C	200's DIGIT
4	DP 1XX.X	D	HOLD
5	OVERLOAD	E	POLARITY
6	40's DIGIT	F	80's DIGIT
7	20's DIGIT	H	10's DIGIT
8	DIGITAL GRD	J	POWER SUPPLY GND
9*	REF IN (2010/R ONLY)	K	STATUS
10	REF OUT	L	3's DIGIT
11	CLOCK OUT	M	1's DIGIT
12	4's DIGIT	N	+5V POWER INPUT
13	ANALOG IN	P	2's DIGIT
14	ANALOG GRD	R	LEADING ZERO SUPPRESSION
15	DP 1X.XX	S	DP 1.XXX

*WHEN IT IS DESIRED TO USE THE AD2010/F INTERNAL 200mV REFERENCE, EXTERNALLY CONNECT PIN "9" TO PIN "10". "REF IN" NOT PROTECTED AGAINST OVERLOAD.
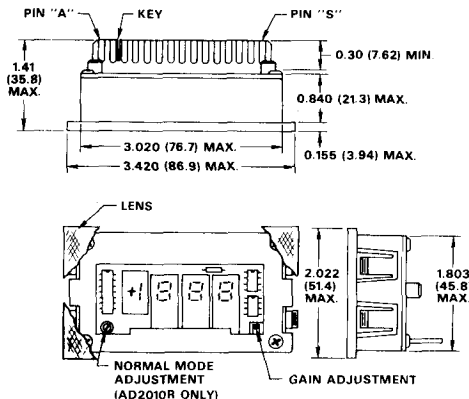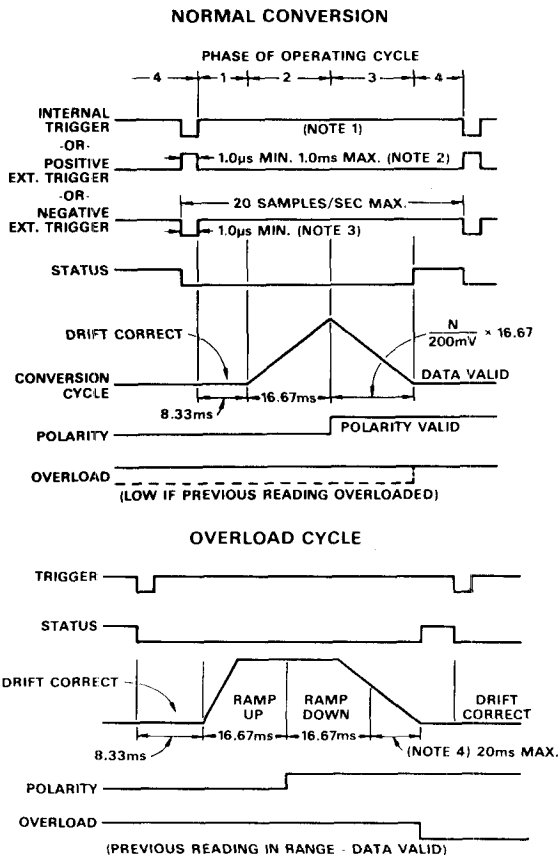
Figure 5. AD2010 Connector Pin Designations

PIN "A"   KEY   PIN "S"

1.41 (35.8) MAX.   0.30 (7.62) MIN
0.840 (21.3) MAX.

3.020 (76.7) MAX.
3.420 (86.9) MAX.   0.155 (3.94) MAX.

LENS

2.022 (51.4) MAX.   1.803 (45.8) MAX.

NORMAL MODE ADJUSTMENT (AD2010R ONLY)   GAIN ADJUSTMENT

Figure 6. Overall Dimensions
All dimensions are given in inches and (mm).

NORMAL CONVERSION

PHASE OF OPERATING CYCLE
4 — 1 — 2 — 3 — 4

INTERNAL TRIGGER   (NOTE 1)
-OR-
POSITIVE EXT. TRIGGER   1.0µs MIN. 1.0ms MAX. (NOTE 2)
-OR-
NEGATIVE EXT. TRIGGER   20 SAMPLES/SEC MAX.
    1.0µs MIN. (NOTE 3)

STATUS

DRIFT CORRECT $\frac{N}{200mV} \times 16.67$

CONVERSION CYCLE   DATA VALID
8.33ms   16.67ms

POLARITY   POLARITY VALID

OVERLOAD
(LOW IF PREVIOUS READING OVERLOADED)

OVERLOAD CYCLE

TRIGGER

STATUS

DRIFT CORRECT   RAMP UP   RAMP DOWN   DRIFT CORRECT
8.33ms   16.67ms 16.67ms   (NOTE 4) 20ms MAX.

POLARITY

OVERLOAD
(PREVIOUS READING IN RANGE - DATA VALID)

NOTES:
1. The internal trigger rate is 4 conversions/sec.
2. A logic "0" applied to the "HOLD" input (pin D) disables the internal trigger. A positive pulse of 1ms max will initiate conversion. The "status" output may be used in this way for automatic triggering.
3. With the internal trigger disabled a negative pulse applied to the "external trigger" (pin 1) will initiate conversion.
4. Total ramp down time dependent on extent of overload (additional 20ms max).

Figure 7. AD2010 Timing Diagram